WIDEBAND FIXED-GAIN AMPLIFIER

FEATURES

- Fixed-Gain Amplifier, 5 V/V (14 dB)
- Wide Bandwidth: 2.4 GHz
- High Slew Rate: 5500 V/μs
- Low Total Input Referred Noise: 2.8 nV/√Hz
- Low Distortion
  - HD_3: -86 dBc at 30 MHz
  - HD_3: -81 dBc at 70 MHz
  - IMD_3: -88 dBc at 100 MHz
  - OIP_3: 39 dBm at 100 MHz
  - IMD_3: -73 dBc at 300 MHz
  - OIP_3: 32 dBm at 300 MHz
- High Output Drive: ±180 mA
- Power Supply Voltage: 3 V or 5 V

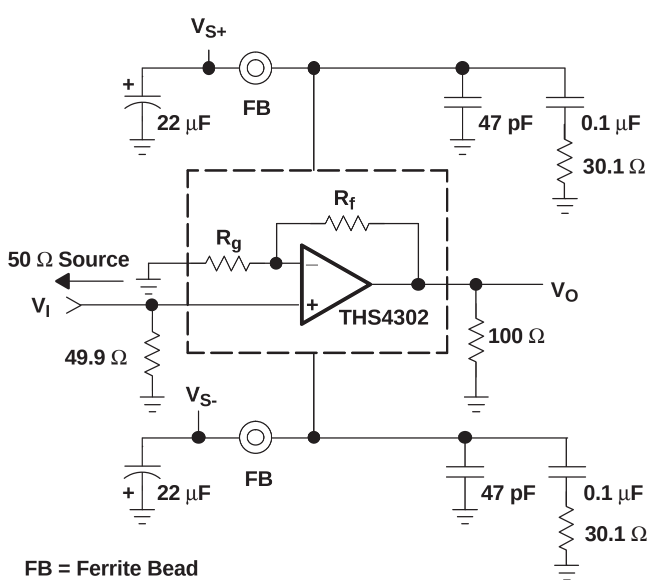
APPLICATIONS

- Wideband Signal Processing
- Wireless Transceivers
- IF Amplifier
- ADC Preamplifier
- DAC Output Buffers
- Test, Measurement, and Instrumentation
- Medical and Industrial Imaging

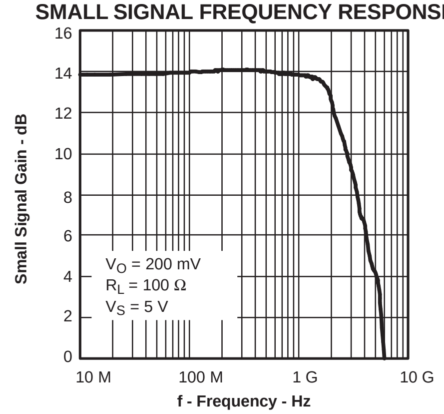
DESCRIPTION

The THS4302 device is a wideband, fixed-gain amplifier that offers high bandwidth, high slew rate, low noise, and low distortion. This combination of specifications enables analog designers to transcend current performance limitations and process analog signals at much higher speeds than previously possible with closed-loop, complementary amplifier designs. This device is offered in a 16-pin leadless package and incorporates a power-down mode for quiescent power savings.

APPLICATION CIRCUIT



SMALL SIGNAL FREQUENCY RESPONSE



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATING

over operating free-air temperature range unless otherwise noted [(1)]

	UNIT
Supply voltage, V_S	6 V
Input voltage, V_I	$\pm V_S$
Output current, I_O	200 mA
Continuous power dissipation	See Dissipation Rating Table
Maximum junction temperature, T_J	150°C
Maximum junction temperature, continuous operation, long term reliability, T_J [(2)]	125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

(1) The absolute maximum temperature under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V_{CC} (V_{S+} and V_{S-})	Dual supply	±1.5	±2.5	V
	Single supply	3	5	
Common-mode input voltage range		V_{S-} +1	V_{S+} -1	V

PACKAGE DISSIPATION RATINGS

PACKAGE	θ_{JC}(°C/W)	θ_{JA}(°C/W) [(1)]	POWER RATING [(2)]	
			$T_A \leq 25°C$	$T_A = 25°C$
RGT (16) [(3)]	2.4	39.5	3.16	1.65 W

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long term reliability.
(3) The THS4302 device may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which can permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the PowerPAD thermally enhanced package.

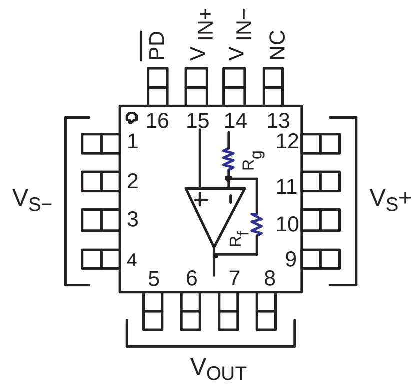
AVAILABLE OPTIONS

INTERNAL FIXED GAIN RESISTOR VALUES (+5)		PACKAGED DEVICES	PACKAGE TYPE [(1)]	TRANSPORTATION MEDIA, QUANTITY
R_G	R_F	THS4302RGTT	Leadless (RGT-16)	Tape and Reel, 250
50 Ω	200 Ω	THS4302RGTR		Tape and Reel, 3000

(1) The PowerPAD is electrically isolated from all other pins.

PIN ASSIGNMENTS

RGT PACKAGE
TOP VIEW



NC = No connect

ELECTRICAL CHARACTERISTICS

THS4302 (Gain = +5 V/V) Specifications: V_S = 5 V, R_L = 100 Ω, (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TYP	OVERTEMPERATURE				
			25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	MIN/ TYP/ MAX
AC PERFORMANCE								
Small signal bandwidth	G = +5, V_O = 200 mV_{RMS}		2.4				GHz	Typ
Gain bandwidth product			12				GHz	Typ
Full-power bandwidth	G = +5, V_O = 2 Vpp		875				MHz	Typ
Slew rate	G = +5, V_O = 2 V Step		5500				V/μs	Min
Harmonic distortion								
Second harmonic distortion	G = +5, V_O = 1 V_{PP}, f = 70 MHz	R_L = 100 Ω	-66				dBc	Typ
		R_L = 1 kΩ	-75				dBc	
Third harmonic distortion		R_L = 100 Ω	-81				dBc	Typ
		R_L = 1 kΩ	-85				dBc	
Third order intermoduation (IMD_3)	V_O = 1 V_{PP} envelope, 200 kHz tone spacing	f_c = 100 MHz	-88				dBc	Typ
		f_c = 300 MHz	-73				dBc	
Third order output intercept (OIP_3)	V_O = 1 V_{PP}, 200 kHz tone spacing	f_c = 100 MHz	39				dBm	Typ
		f_c = 300 MHz	32				dBm	
Total input referred noise	f = 1 MHz		2.8				nV/√Hz	Typ
Noise figure			16				dB	Typ
DC PERFORMANCE								
Voltage gain	V_I = ±50 mV, V_{CM} = 2.5 V		5	4.95	4.95	4.95	V/V	Min
			5	5.05	5.05	5.05	V/V	Max
Input offset voltage	V_{CM} = 2.5 V		2	4.25	5.25	5.25	mV	Max
Average offset voltage drift	V_{CM} = 2.5 V				±20	±20	μV/°C	Typ
Input bias current	V_{CM} = 2.5 V		7	10	13	15	μA	Max
Average bias current drift	V_{CM} = 2.5 V				±55	±55	nA/°C	Typ

ELECTRICAL CHARACTERISTICS (continued)

THS4302 (Gain = +5 V/V) Specifications: V_S = 5 V, R_L = 100 Ω, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVERTEMPERATURE				
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	MIN/ TYP/ MAX
INPUT CHARACTERISTICS							
Common-mode input range		0.5/4.5	1/4	1.1/3.9	1.2/3.8	V	Min
Common-mode rejection ratio	V_{CM} = 2 V to 3 V	60	52	50	50	dB	Min
Input resistance	Noninverting input	1.6				MΩ	Typ
Input capacitance	Noninverting input	1				pF	Max
OUTPUT CHARACTERISTICS							
Output voltage swing		1/4	1.1/3.9	1.2/3.8	1.2/3.8	V	Min
Output current (sourcing)	R_L = 5 Ω	180	170	165	160	mA	Min
Output current (sinking)	R_L = 5 Ω	180	170	165	160	mA	Min
Output impedance	f = 10 MHz	0.2				Ω	Typ
POWER SUPPLY							
Operating voltage		5	5.5	5.5	5.5	V	Max
Maximum quiescent current		37	42	46	48	mA	Max
Minimum quiescent current		37	32	29	26	mA	Min
Power supply rejection ratio (PSRR +)	V_{S+} = 5 V to 4.5 V, V_{S-} = 0 V	60	54	52	51	dB	Min
Power supply rejection ratio (PSRR -)	V_{S+} = 5 V, V_{S-} = 0 V to 0.5 V	75	65	64	62	dB	Min
POWER-DOWN CHARACTERISTICS							
Maximum power-down current	$\overline{PD}$ = 0 V	0.8	1.0	1.1	1.2	mA	Max
Power-on voltage threshold		1.1	1.5			V	Min
Power-down voltage threshold		1.1	0.9			V	Max
Turnon time delay, $t_{d(on)}$	50% of final value	6				µs	Typ
Turnoff time delay, $t_{d(off)}$	50% of final value	5				µs	Typ
Input impedance		100				kΩ	Typ
Output impedance	f = 100 kHz	250				Ω	Typ

TYPICAL CHARACTERISTICS

Table of Graphs (5 V)

	FIGURE
S-Parameter vs Frequency	1
Small signal frequency response	2
Large signal frequency response	3
Slew rate vs Output voltage	4
Harmonic distortion vs Frequency	5, 6, 7, 8
Harmonic distortion vs Output voltage swing	9
Second-order intermodulation distortion vs Frequency	10
Second-order intercept point vs Frequency	11
Third order intermodulation distortion vs Frequency	12
Third-order intercept point vs Frequency	13
Voltage and current noise vs Frequency	14
Settling time	15, 16
Quiescent current vs Supply voltage	17
Output voltage vs Load resistance	18
Capacitive load frequency response	19
Gain vs Case temperature	20
Rejection ratios vs Frequency	21
Rejection ratios vs Case temperature	22
Common-mode rejection ratio vs Input common-mode range	23
Input offset voltage vs Case temperature	24
Positive input bias current vs Case temperature	25
Small signal transient response	26
Large signal transient response	27
Overdrive recovery	28
Closed-loop output impedance vs Frequency	29
Power-down quiescent current vs Supply voltage	30
Power-down output impedance vs Frequency	31
Turnon and turnoff delay times	32
Power-down S-Parameter vs Frequency	33

Table of Graphs (3 V)

	FIGURE
Small signal frequency response	34
Large signal frequency response	35
Slew rate vs Output voltage	36
Output voltage vs Load resistance	37
Capacitive load frequency response	38
Gain vs Case temperature	39
S - Parameter vs Frequency	40
Input offset voltage vs Case temperature	41
Positive input bias current vs Case temperature	42
Overdrive recovery	43

TEXAS INSTRUMENTS
www.ti.com

Typical Test Data

S-Parameter (Measured using standard THS4302EVM, edge number 6443548, with V_S = 5 V in a 50-Ω test system)								
Frequency MHz	S11 (dB)	S11 (Ang)	S21 (dB)	S21 (Ang)	S12 (dB)	S12 (Ang)	S22 (dB)	S22 (Ang)
1	-55.86328	-3.728516	14.10889	-0.093384	-96.26953	20.78809	-70.32422	122.5
2	-55.75781	-4.832764	14.11621	-0.109863	-98.18359	-120.6758	-65.65234	97.16016
10	-53.0293	-29.01563	14.11035	-0.350189	-78.10156	121.2148	-52.01953	73.91406
50	-42.92383	-82.44141	14.16309	-1.682312	-61.82813	75	-45.27539	142.0391
100	-37.35156	-97.42188	14.34766	-4.422119	-56.37891	61.26367	-31.04981	115.4414
150	-35.64258	-105.9063	14.38428	-7.657471	-54.44336	53.0957	-26.75098	98.26172
200	-33.27344	-111.1133	14.42041	-10.49512	-53.72852	34.22656	-25.3418	85.07031
250	-32.18945	-114.2891	14.39209	-13.63135	-53.55273	31.70508	-24.14844	77.09766
300	-30.92578	-114.4297	14.40918	-17.17871	-53.94727	21.56934	-23.53613	72.94531
350	-30.29492	-113.9727	14.38477	-19.34375	-54.23828	19.45508	-22.99512	70.63281
400	-29.11816	-113.5313	14.38184	-23.08594	-55.13281	16.29395	-22.13379	72.0625
450	-28.44141	-116	14.35645	-25.62305	-56.33594	14.38232	-21.45215	71.90234
500	-27.50977	-114.082	14.36035	-28.69922	-58.48828	12.0708	-20.56641	74.21094
550	-26.51856	-112.25	14.3208	-32.48047	-63.26367	3.492187	-19.71094	74.85938
600	-26.01856	-113.6719	14.30713	-34.17773	-67.62109	27.33594	-19.2959	75.58984
700	-24.03613	-115.8984	14.23242	-39.5918	-68.02734	172.2422	-17.80078	77.79297
800	-21.97559	-117.4922	14.1665	-47.05664	-55.4082	171.0703	-15.81494	77.22266
900	-20.40137	-120.7305	14.11133	-51.92969	-50.38477	168.8125	-14.38965	76.04297
1000	-18.70313	-123.4023	14.06006	-57.80078	-46.64453	163.1016	-12.91406	73.89063
1250	-15.14893	-134.7031	13.93872	-75.02344	-40.19141	152.5313	-9.994141	65.77734
1500	-12.66602	-149.0625	13.74683	-88.4375	-35.73438	139.7109	-7.968018	55.74414
1750	-11.48975	-168.9922	12.97827	-110.2852	-31.94531	112.5	-6.750977	40.24414
2000	-11.68311	-169.8203	12.18066	-123.043	-34.46094	84.83984	-7.211182	31.3877

TYPICAL THS4302 CHARACTERISTICS (5 V)

S-PARAMETER vs FREQUENCY

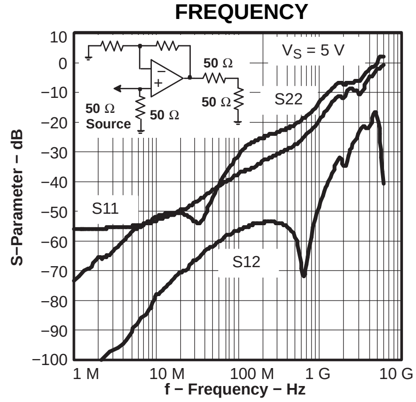


Figure 1.

SMALL SIGNAL FREQUENCY RESPONSE

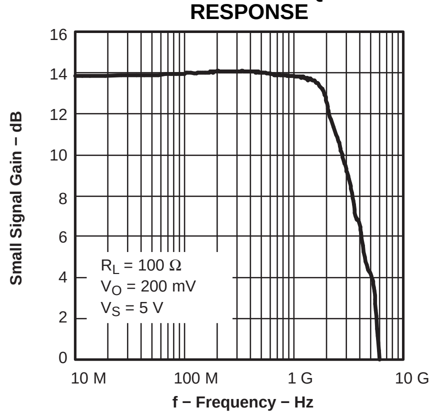


Figure 2.

LARGE SIGNAL FREQUENCY RESPONSE

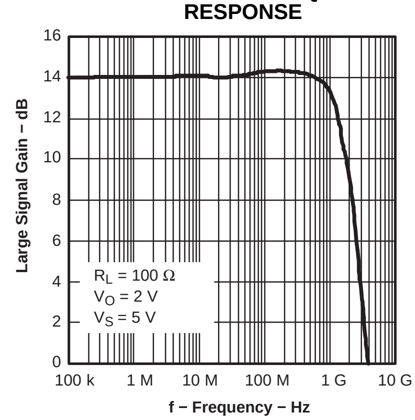


Figure 3.

TYPICAL THS4302 CHARACTERISTICS (5 V) (continued)

SLEW RATE vs OUTPUT VOLTAGE

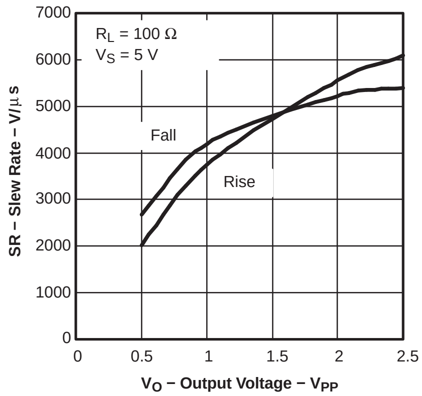


Figure 4.

HARMONIC DISTORTION vs FREQUENCY

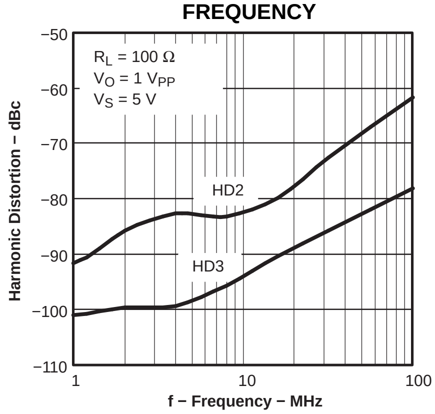


Figure 5.

HARMONIC DISTORTION vs FREQUENCY

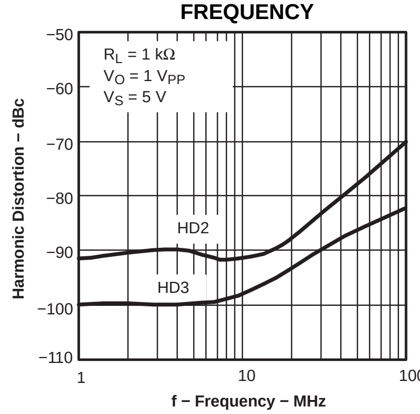


Figure 6.

HARMONIC DISTORTION vs FREQUENCY

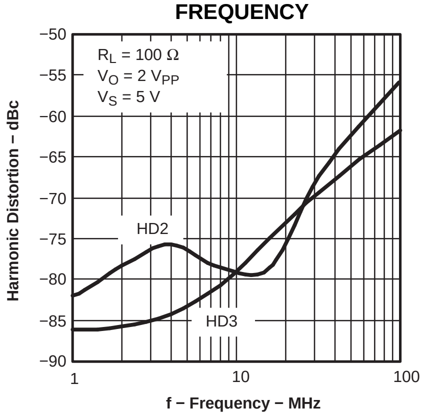


Figure 7.

HARMONIC DISTORTION vs FREQUENCY

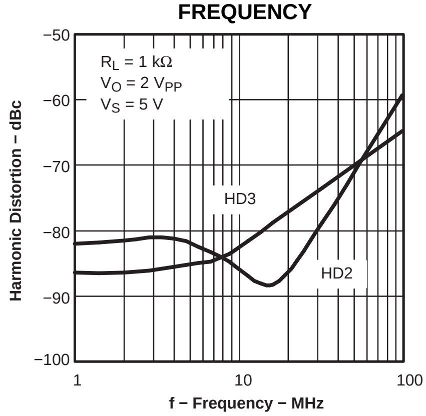


Figure 8.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

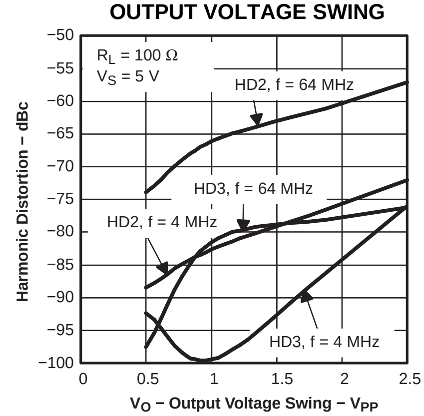


Figure 9.

SECOND-ORDER INTERMODULATION DISTORTION vs FREQUENCY

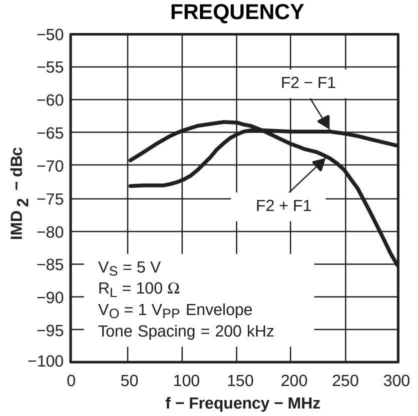


Figure 10.

SECOND-ORDER OUTPUT INTERCEPT POINT vs FREQUENCY

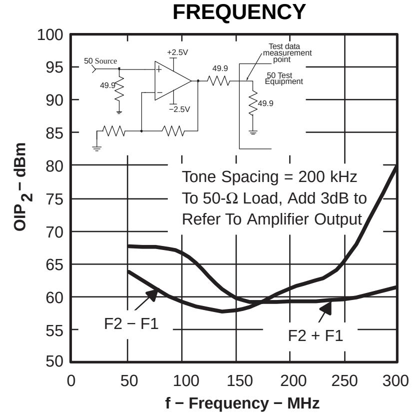


Figure 11.

THIRD-ORDER INTERMODULATION DISTORTION vs FREQUENCY

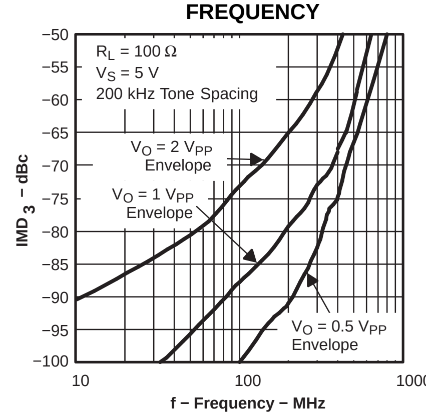


Figure 12.

TEXAS INSTRUMENTS
www.ti.com

TYPICAL THS4302 CHARACTERISTICS (5 V) (continued)

THIRD-ORDER OUTPUT INTERCEPT POINT vs FREQUENCY

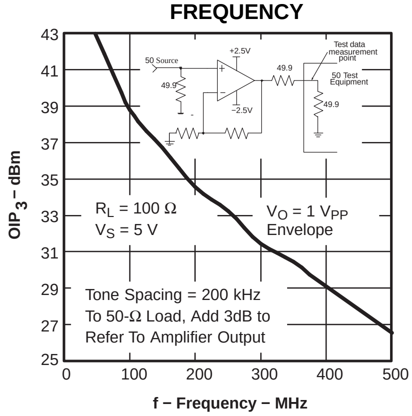


Figure 13.

VOLTAGE AND CURRENT NOISE vs FREQUENCY

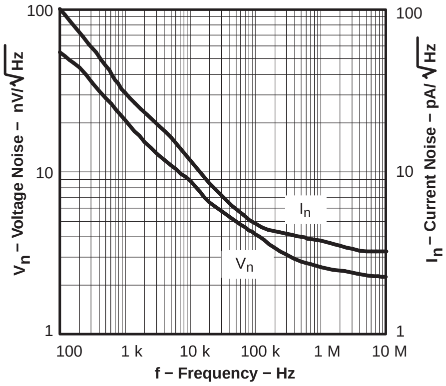


Figure 14.

SETTLING TIME

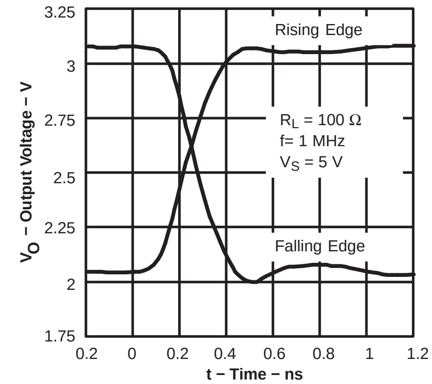


Figure 15.

SETTLING TIME

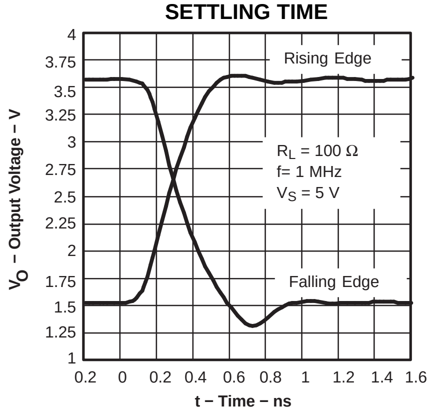


Figure 16.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

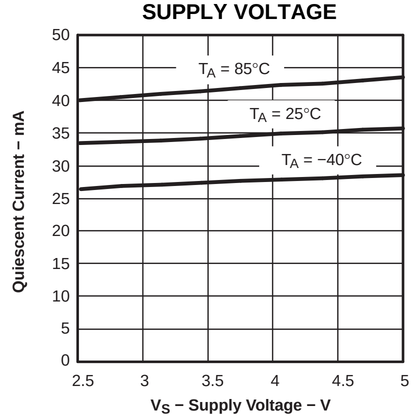


Figure 17.

OUTPUT VOLTAGE vs LOAD RESISTANCE

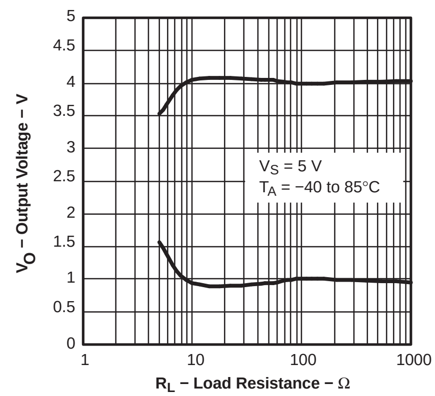


Figure 18.

CAPACITIVE LOAD FREQUENCY RESPONSE

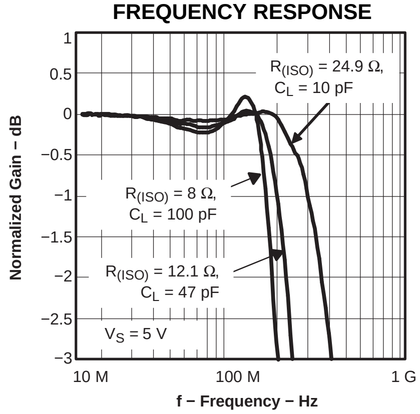


Figure 19.

GAIN vs CASE TEMPERATURE

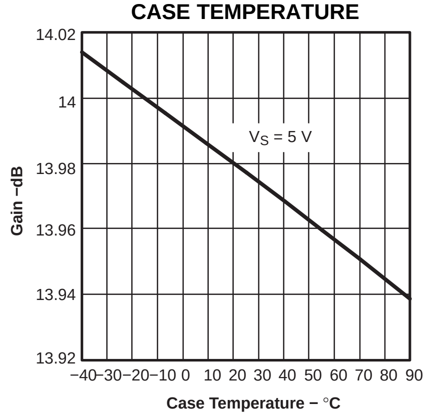


Figure 20.

REJECTION RATIOS vs FREQUENCY

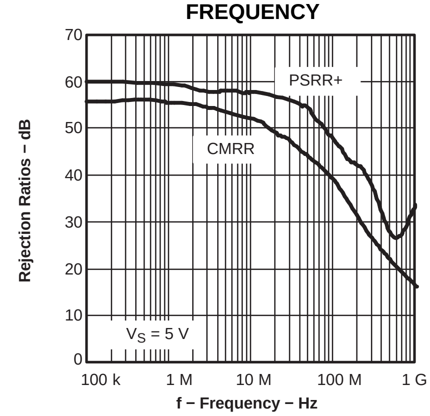


Figure 21.

TYPICAL THS4302 CHARACTERISTICS (5 V) (continued)

REJECTION RATIOS vs CASE TEMPERATURE

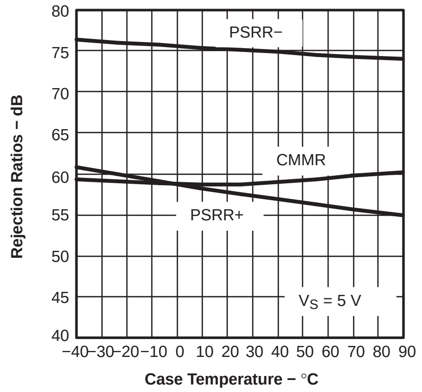


Figure 22.

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

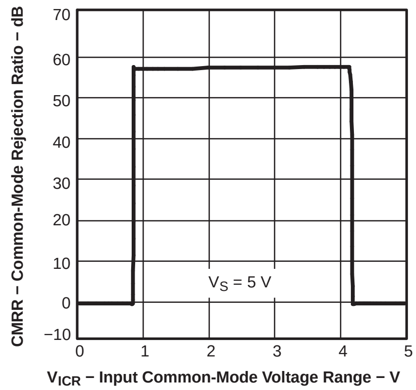


Figure 23.

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

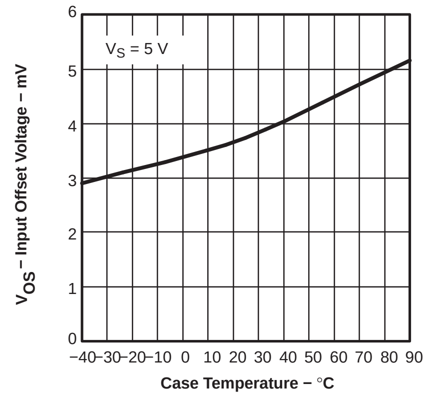


Figure 24.

POSITIVE INPUT BIAS CURRENT vs CASE TEMPERATURE

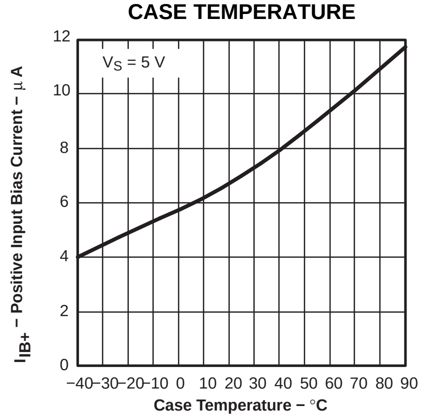


Figure 25.

SMALL SIGNAL TRANSIENT RESPONSE

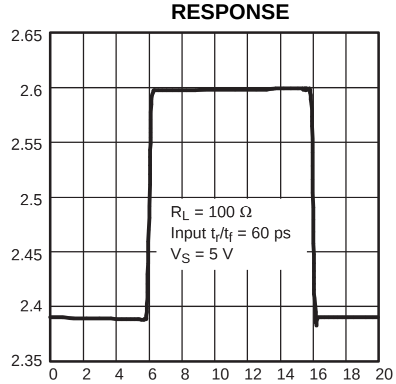


Figure 26.

LARGE SIGNAL TRANSIENT RESPONSE

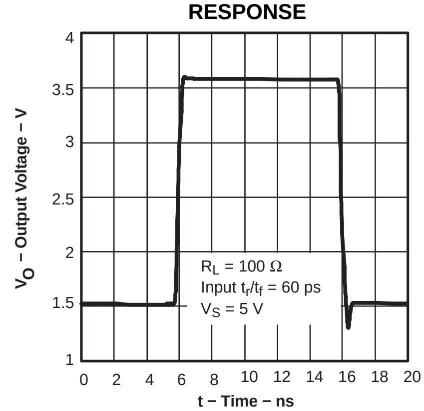


Figure 27.

OVERDRIVE RECOVERY

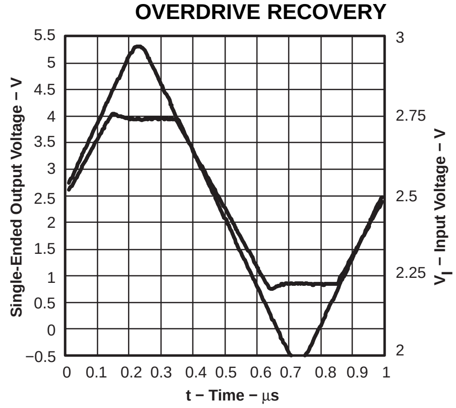


Figure 28.

OUTPUT IMPEDANCE vs FREQUENCY

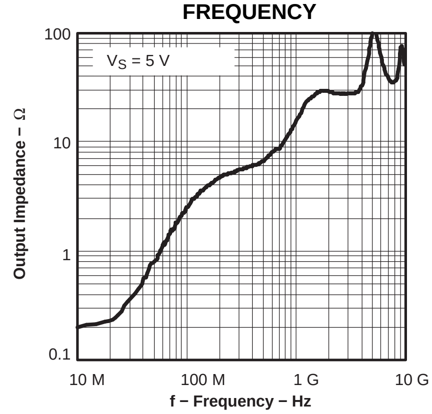


Figure 29.

POWER-DOWN QUIESCENT CURRENT vs SUPPLY VOLTAGE

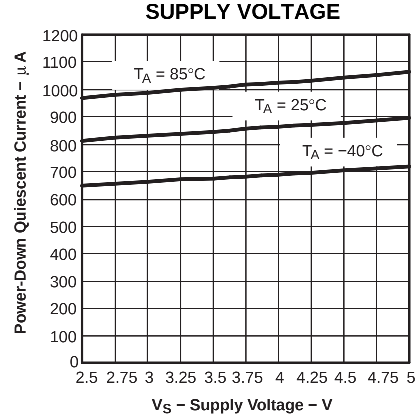


Figure 30.

TYPICAL THS4302 CHARACTERISTICS (5 V) (continued)

POWER-DOWN OUTPUT IMPEDANCE vs FREQUENCY

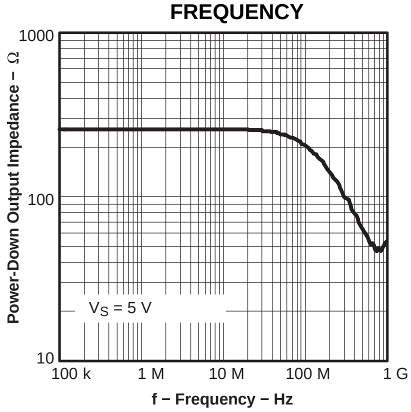


Figure 31.

TURNON AND TURNOFF TIMES DELAY TIME

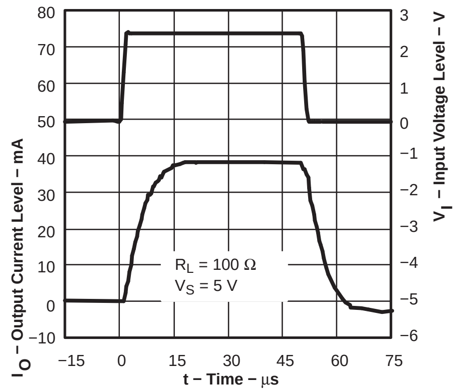


Figure 32.

POWER-DOWN S-PARAMETER vs FREQUENCY

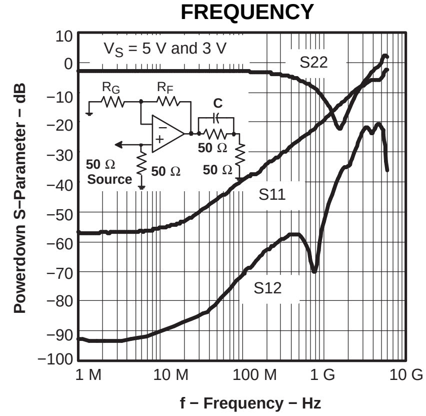


Figure 33.

TYPICAL THS4302 CHARACTERISTICS (3 V)

SMALL SIGNAL FREQUENCY RESPONSE

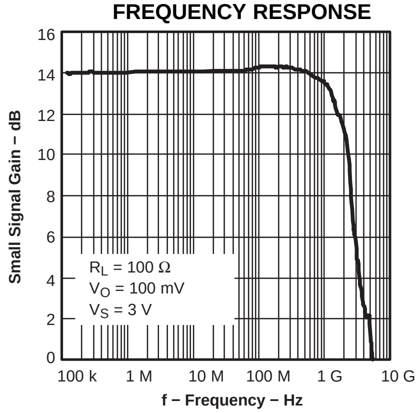


Figure 34.

LARGE SIGNAL FREQUENCY RESPONSE

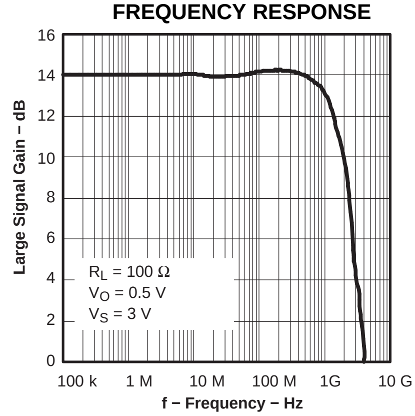


Figure 35.

SLEW RATE vs OUTPUT VOLTAGE

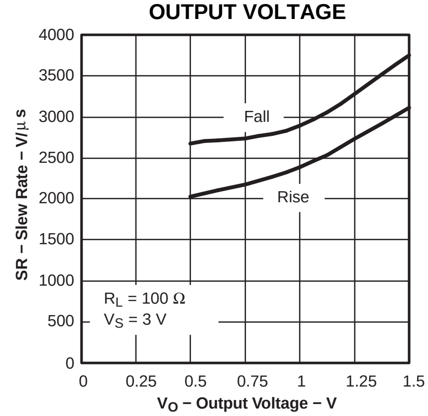


Figure 36.

OUTPUT VOLTAGE vs LOAD RESISTANCE

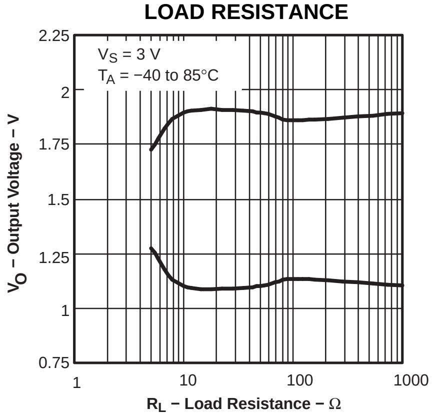


Figure 37.

CAPACITIVE LOAD FREQUENCY RESPONSE

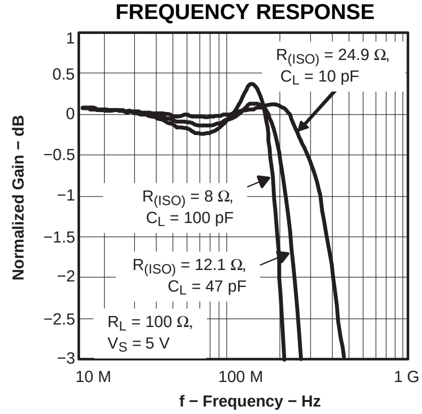


Figure 38.

GAIN vs CASE TEMPERATURE

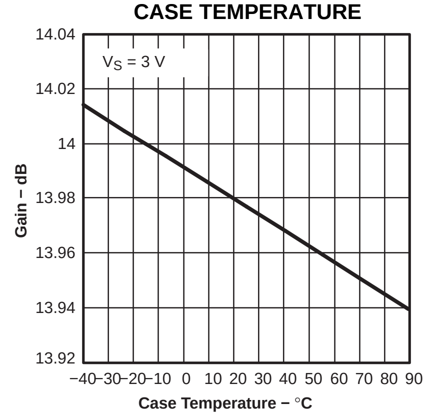


Figure 39.

TYPICAL THS4302 CHARACTERISTICS (3 V) (continued)

S-PARAMETER vs FREQUENCY

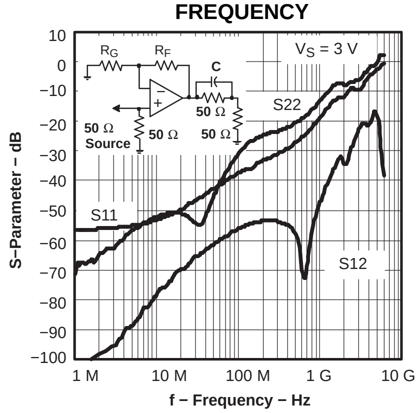


Figure 40.

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

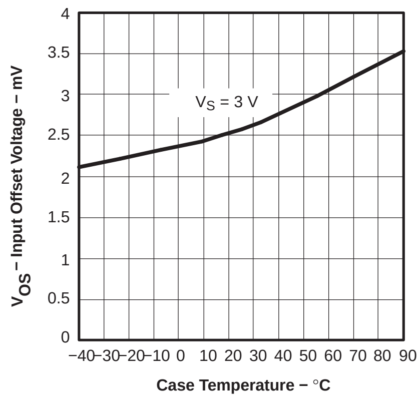


Figure 41.

POSITIVE INPUT BIAS CURRENT vs CASE TEMPERATURE

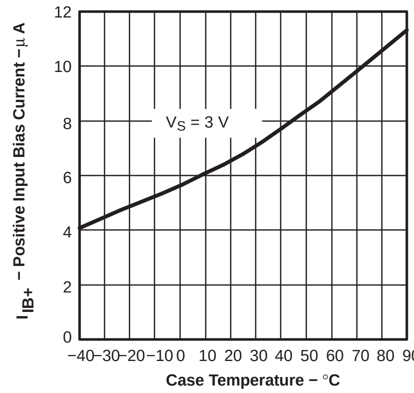


Figure 42.

OVERDRIVE RECOVERY

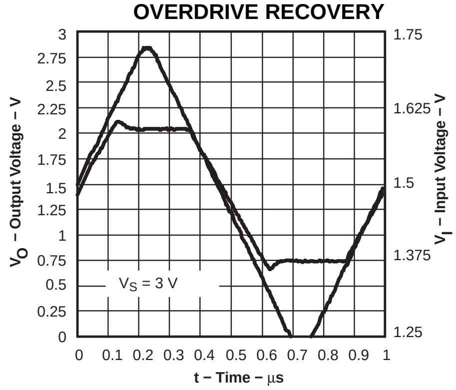


Figure 43.

APPLICATION INFORMATION

High-Speed Operational amplifiers

The THS4302 fixed-gain operational amplifier set new performance levels, combining low distortion, high slew rates, low noise, and a gain bandwidth in excess of 2 GHz. To achieve the full performance of the amplifier, careful attention must be paid to printed-circuit board layout and component selection.

In addition, the devices provide a power-down mode with the ability to save power when the amplifier is inactive.

Applications Section Contents

- Wideband, Noninverting Operation
- Single Supply Operation
- Saving Power With Power-Down Functionality
- Driving an ADC With the THS4302
- Driving Capacitive Loads
- Power Supply Decoupling Techniques and Recommendations
- Board Layout
- Printed-Circuit Board Layout Techniques for Optimal Performance
- PowerPAD Design Considerations
- PowerPAD PCB Layout Considerations
- Thermal Analysis
- Design Tools
- Evaluation Fixtures and Application Support Information
- Additional Reference Material
- Mechanical Package Drawings

WIDEBAND, NONINVERTING OPERATION

The THS4302 is a fixed-gain voltage feedback operational amplifier, with power-down capability, designed to operate from a single 3-V to 5-V power supply.

Figure 44 is the noninverting gain configuration used to demonstrate the typical performance curves. Most of the curves were characterized using signal sources with 50-Ω source impedance, and with measurement equipment presenting a 50-Ω load impedance. In Figure 44, the 49.9-Ω shunt resistor at the V_{IN} terminal matches the source impedance of the test generator. The 50-Ω series resistor at the V_O terminal in addition to the 50-Ω load impedance of the test equipment, provides a 100-Ω load. The total 100-Ω load at the output, combined with the 250-Ω total feedback network load, presents the THS4302 with an effective output load of 71 Ω for the circuit of Figure 44.

INTERNAL FIXED RESISTOR VALUES

DEVICE	GAIN (V/V)	R_f	R_g
THS4302	+5	200	50

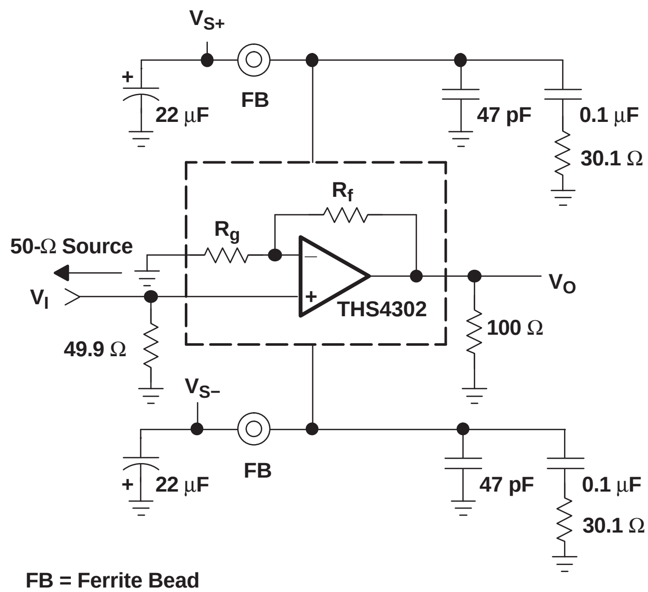


Figure 44. Wideband, Noninverting Gain Configuration

SINGLE SUPPLY OPERATION

The THS4302 is designed to operate from a single 3-V to 5-V power supply. When operating from a single power supply, care must be taken to ensure the input signal and amplifier are biased appropriately to allow for the maximum output voltage swing. The circuits shown in Figure 45 demonstrate methods to configure an amplifier in a manner conducive for single supply operation.

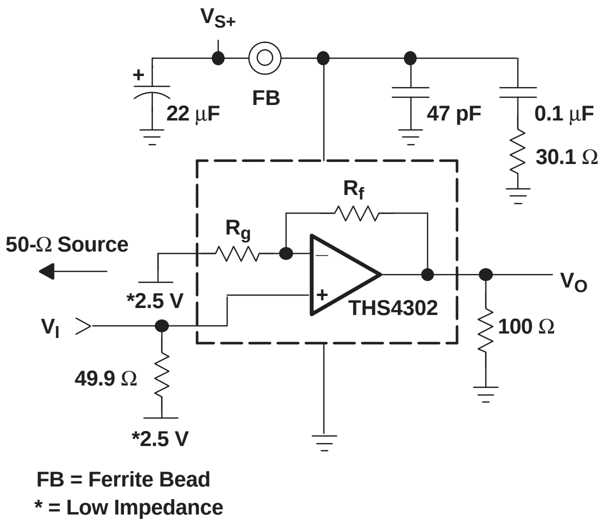


Figure 45. DC-Coupled Single Supply Operation

Saving Power With Power-Down Functionality

The THS4302 features a power-down pin ($\overline{PD}$) which lowers the quiescent current from 37 mA down to 800 µA, ideal for reducing system power.

The power-down pin of the amplifier defaults to the positive supply voltage in the absence of an applied voltage, putting the amplifier in the power-on mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be driven towards the negative rail. The threshold voltages for power-on and power-down are relative to the supply rails and given in the specification tables. Above the *Enable Threshold Voltage*, the device is on. Below the *Disable Threshold Voltage*, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high-impedance output. In other words, the power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach 50% of the nominal quiescent current. The time delays are on the order of microseconds because the amplifier moves in and out of the linear mode of operation in these transitions.

APPLICATION CIRCUITS

Driving an Analog-to-Digital Converter With the THS4302

The THS4302 amplifier can be used to drive high-performance analog-to-digital converters. Two example circuits are presented below.

The first circuit uses a wideband transformer to convert a single-ended input signal into a differential signal. The amplified signal from the output of the THS4302 is fed through a low-pass filter, via an isolation resistor and an ac-coupling capacitor, to the transformer.

For applications without signal content at dc, this method of driving ADCs is useful. Where dc information content is required, the THS4500 family of fully differential amplifiers may be applicable.

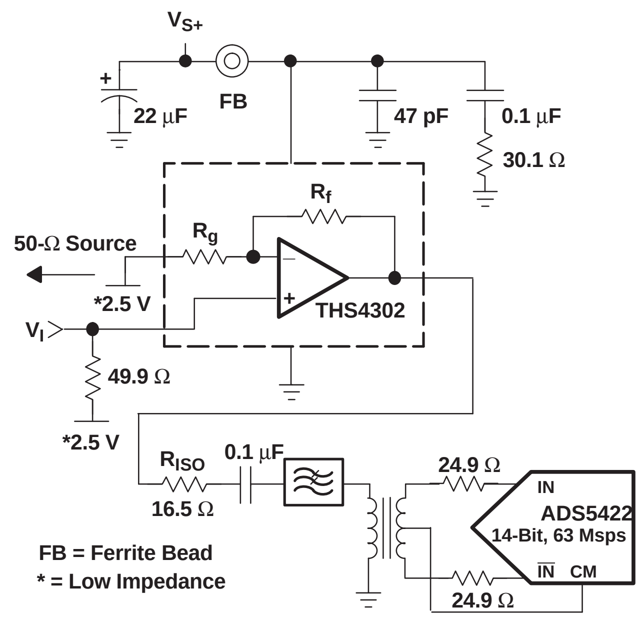


Figure 46. Driving an ADC Via a Transformer

The second circuit depicts single-ended ADC drive. While not recommended for optimum performance using converters with differential inputs, satisfactory performance can sometimes be achieved with single-ended input drive. An example circuit is shown here for reference.

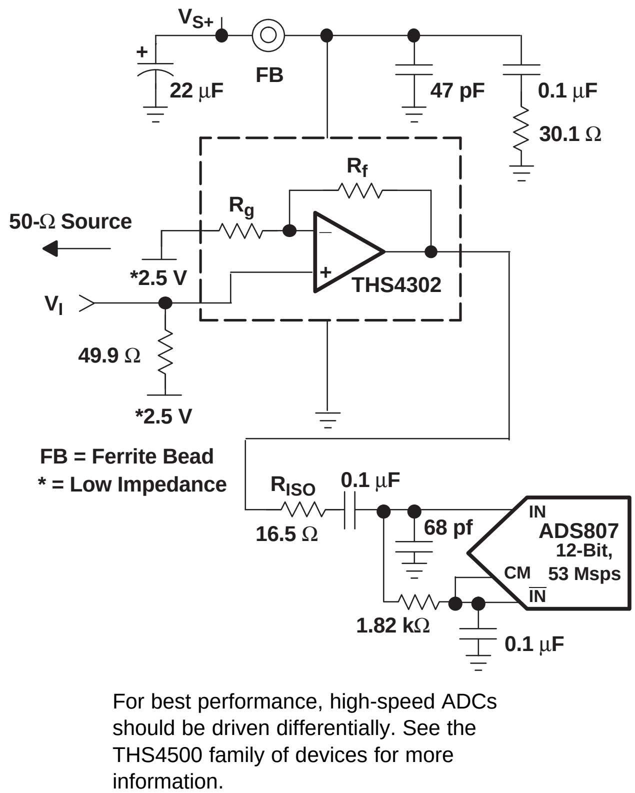


Figure 47. Driving an ADC With a Single-Ended Input

Driving Capacitive Loads

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter, including additional external capacitance, which may be recommended to improve A/D linearity. High-speed amplifiers like the THS4302 can be susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. When the primary considerations are frequency response flatness, pulse response fidelity, or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load.

The Typical Characteristics show the recommended isolation resistor vs capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2 pF can begin to degrade the performance of the THS4302. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the THS4302 output pin (see Board Layout Guidelines).

The criterion for setting this $R_{(ISO)}$ resistor is a maximum bandwidth, flat frequency response at the load.

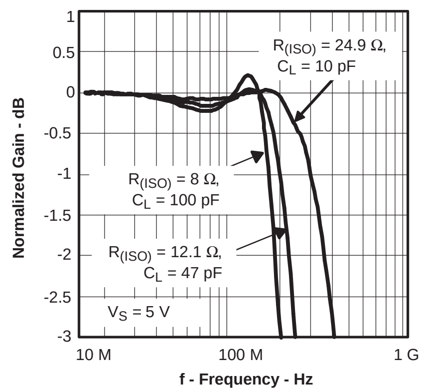


Figure 48. Driving Capacitive Loads

Power Supply Decoupling Techniques and Recommendations

Power supply decoupling is a critical aspect of any high-performance amplifier design process. Careful decoupling provides higher quality ac performance (most notably improved distortion performance). The following guidelines ensure the highest level of performance.

1. Place decoupling capacitors as close to the power supply inputs as possible, with the goal of minimizing the inductance of the path from ground to the power supply. Inductance in series with the bypass capacitors will degrade performance. Note that a narrow lead or trace has about 0.8 nH of inductance for every millimeter of length. Each printed-circuit board (PCB) via also has between 0.3 and 0.8 nH depending on length and diameter. For these reasons, it is recommended to use a power supply trace about the width of the package for each power supply lead to the capacitors, and 3 or more vias to connect the capacitors to the ground plane.
2. Placement priority should put the smallest valued capacitors closest to the device.
3. Solid power planes can lead to PCB resonances

when they are not properly terminated to the ground plane over the area and along the perimeter of the power plane by high frequency capacitors. Doing so ensures that there are no power plane resonances in the needed frequency range. Values used are in the range of 2 pF - 50 pF, depending on the frequencies to be suppressed, with numerous vias for each. Using 0402 or smaller component sizes is recommended. An approximate expression for the resonant frequencies associated with a length of one of the power plane dimensions is given in the following equation. Note that a power plane of arbitrary shape can have a number of resonant frequencies. A power plane without distributed capacitors and with active parts near the center of the plane usually has *n* even (≥ 2) due to the half wave resonant nature of the plane.

$$\text{frequency}_{res} \approx \frac{n \times (44\,\text{GHz mm})}{\ell}$$

where:

frequency_{res} = the approximate power plane resonant frequencies in GHz

ℓ = the length of the power plane dimensions in millimeters

n = an integer ($n > 1$) related to the mode of the oscillation

For guidance on capacitor spacing over the area of the ground plane, specify the lowest resonant frequency to be tolerated, then solve using the equation above, with $n = 2$. Use this length for the capacitor spacing. It is recommended that a power plane, if used, be either small enough, or decoupled as described, so that there are no resonances in the frequency range of interest. An alternative is to use a ferrite bead outside the op-amp, high-frequency bypass capacitors to decouple the amplifier, and mid- and high-frequency bypass capacitors, from the power plane. When a trace is used to deliver power, its approximate self-resonance is given by the equation above, substituting the trace length for power plane dimension.

4. Bypass capacitors, because they have a self-inductance, resonate with each other. To achieve optimum transfer characteristics through 2 GHz, it is recommended that the bypass arrangement employed in the prototype board be used. The 30.1-Ω resistor in series with the 0.1-μF capacitor reduces the Q of the resonance of the lumped parallel elements including the 0.1-μF and 47-pF capacitors, and the power supply input of the amplifier. The ferrite bead isolates the low-frequency 22-μF capacitor and power plane from the remainder of the bypass network.
5. By removing the 30.1-Ω resistor and ferrite bead, the frequency response characteristic above 400 MHz may be modified. However, bandwidth, distortion, and transient response remain optimal.
6. Recommended values for power supply decoupling include a bulk decoupling capacitor (22 μF), a ferrite bead with a high self-resonant frequency, a mid-range decoupling capacitor (0.1 μF) in series with a 30.1-Ω resistor, and a high-frequency decoupling capacitor (47 pF).

BOARD LAYOUT

Printed-Circuit Board Layout Techniques for Optimal Performance

Achieving optimum performance with a high frequency amplifier like the THS4302 requires careful attention to board layout parasitics and external component types.

Recommendations that optimize performance include:

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** However, if using a transmission line at the I/O, then place the matching resistor as close to the part as possible. Except for when transmission lines are used, parasitic capacitance on the output and the noninverting input pins can react with the load and source impedances to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground planes and power planes (if used) should be unbroken elsewhere on the board, and terminated as described in the Power Supply Decoupling section.
2. **Minimize the distance (< 0.25”) from the power supply pins to high frequency 0.1-μF decoupling capacitors.** At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Note that each millimeter of a line, that is narrow relative to its length, has ~ 0.8 nH of inductance. The power supply connections should always be decoupled with the recommended capacitors. If not properly decoupled, distortion performance is degraded. Larger (6.8-μF to 22-μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply lines, preferably decoupled from the amplifier and mid- and high-frequency capacitors by a ferrite bead. See the Power Supply Decoupling Techniques section. The larger caps may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board. A very low inductance path should be used to connect the inverting pin of the amplifier to ground. A minimum of 5 vias as close to the part as

possible is recommended.

3. **Careful selection and placement of external components preserves the high frequency performance of the THS4302.** Resistors should be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Axially-leaded parts do not provide good high frequency performance, because they have ~0.8 nH of inductance for every mm of current path length. Again, keep PC board trace length as short as possible. Never use wirewound type resistors in a high frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the terminating resistors, if any, as close as possible to the noninverting and output pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor.
4. **Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs Capacitive Load. Low parasitic capacitive loads (<4 pF) may not need an R_{ISO} because THS4302 amplifiers are nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_{ISO} are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS4302 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case, and set the series resistor value as shown in the plot of R_{ISO} vs Capacitive Load. This does not preserve signal integrity as well as a doubly terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance. A 50-Ω environment is normally not necessary on board as long as the lead lengths are short, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. Uncontrolled impedance traces without double termination results in reflections at each end, and hence, produces PCB resonances. It is recommended that if this approach is used, the trace length be kept short enough to avoid resonances in the band of interest. For guidance on useful lengths, use equation (1) given in the Power Supply Decoupling Techniques section for approximate resonance frequencies vs trace length. This relation provides an upper bound on the resonant frequency, because additional capacitive coupling to the trace from other leads or the ground plane causes extra distributed loading and slows the signal propagation along the trace.
5. **Socketing a high-speed part like the THS4302 is not recommended.** The additional lead length inductance and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS4302 onto the board.

PowerPAD™ DESIGN CONSIDERATIONS

The THS4302 is available in a thermally enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe on which the die is mounted [see Figure 49(a) and Figure 49(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 49(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows both assembly and thermal management in one manufacturing operation.

During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the heretofore awkward mechanical methods of heatsinking.

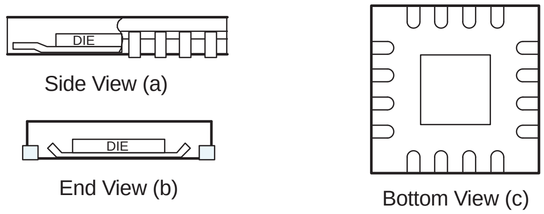


Figure 49. Views of Thermally Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

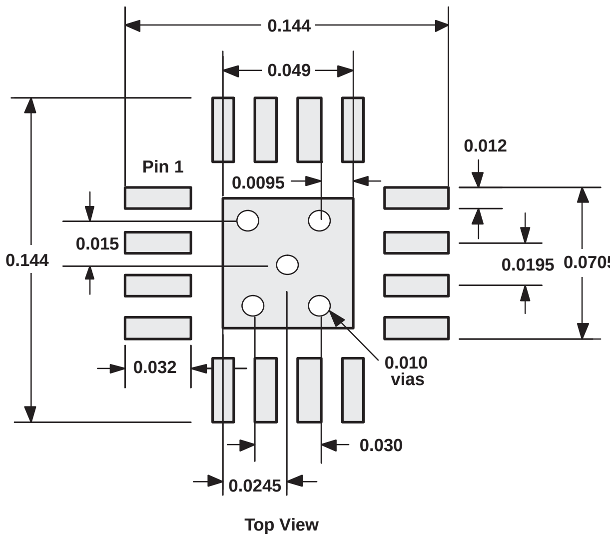


Figure 50. PowerPAD PCB Etch and Via Pattern

PowerPAD™ PCB LAYOUT CONSIDERATIONS

1. Prepare the PCB with a top side etch pattern as shown in Figure 50. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. They holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. They help dissipate the heat generated by the IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This resistance makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the IC PowerPAD package should make their connection to the internal ground plane, with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class AB), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, Θ_{JA} decreases and the heat dissipation capability increases. For a single package, the sum of the RMS output currents and voltages should be used to choose the proper package.

THERMAL ANALYSIS

The THS4302 device does not incorporate automatic thermal shutoff protection, so the designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of 150°C is exceeded.

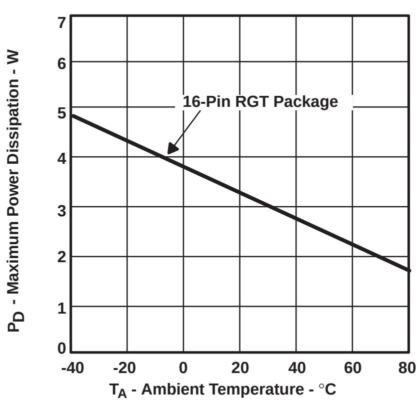
The thermal characteristics of the device are dictated by the package and the PC board. For a given Θ_{JA}, maximum power dissipation for a package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}} \quad (1)$$

where:

P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

The THS4302 is offered in a 16-pin leadless MSOP with PowerPAD. The thermal coefficient for the MSOP PowerPAD package is substantially improved over the traditional packages. Maximum power dissipation levels are depicted in the graph below. The data for the RGT package assumes a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application notes in the *Additional Reference Material* section at the end of the data sheet.



θ_{JA} = 39.5°C/W for 16-Pin MSOP (RGT)
T_J = 150°C, No Airflow

Figure 51. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to consider not only quiescent power dissipation, but also dynamic power dissipation. Often maximum power is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DESIGN TOOLS

Evaluation Fixtures and Application Support Information

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal, an evaluation board has been developed for the THS4302 operational amplifier. The evaluation board is available and easy to use allowing for straight-forward evaluation of the device. This evaluation board can be obtained by ordering through the Texas Instruments Web site, www.ti.com, or through your local Texas Instruments Sales Representative. A schematic for the evaluation board with default component values is shown in Figure 52. Unpopulated footprints are shown to provide insight into design flexibility

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS4500 family of devices is available through the Texas Instruments web site (www.ti.com). The Product Information Center (PIC) is available for design assistance and detailed product information. These models do a good job of predicting small signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

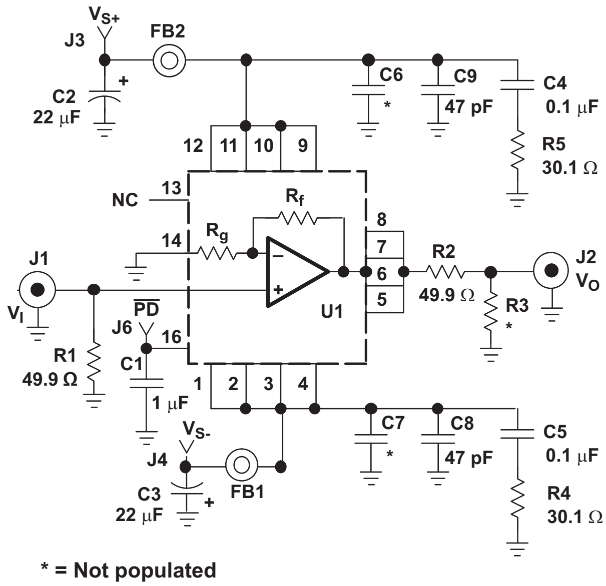


Figure 52. Typical THS4302 EVM Circuit Configuration

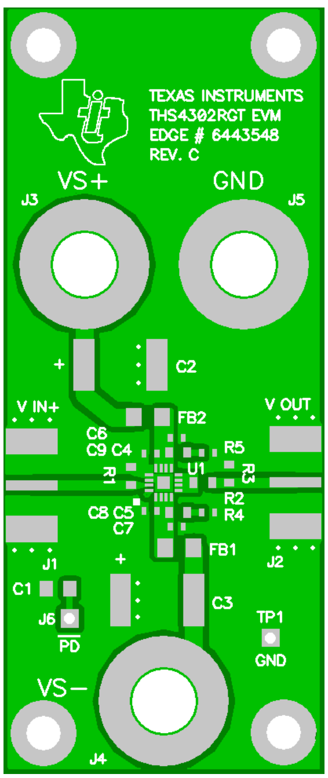


Figure 53. THS4302EVM Layout (Top Layer and Silkscreen Layer)

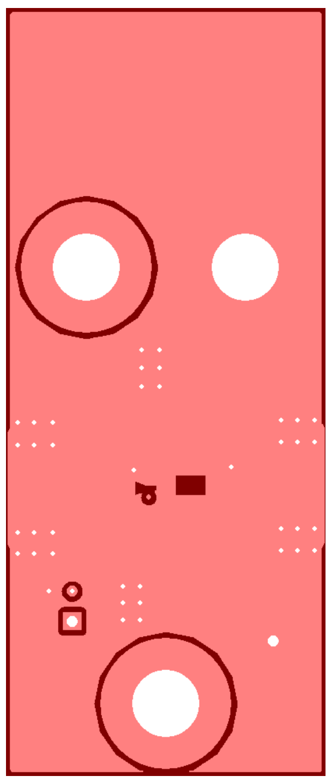


Figure 54. THS4302EVM Board Layout (Ground Layers 2 and 3)

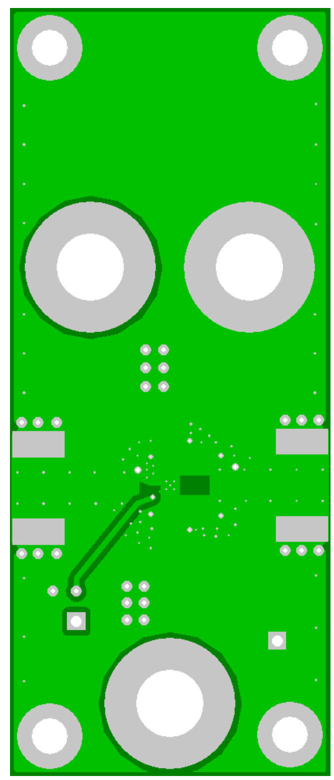


Figure 55. THS4302EVM Board Layout (Bottom Layer)

Table 1. BILL OF MATERIALS - THS4302RGT EVM

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QUANTITY	MANUFACTURER'S PART NUMBER
1	Bead, ferrite, 3 A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00
2	Cap. 22 µF, tantalum, 25 V, 10%	D	C2, C3	2	(AVX) TAJD226K025R
3	Cap. 1 µF, ceramic, 25 V, Y5V	0805	C1	1	(AVX) 08053G105ZAT2A
4	Open	0402	C6, C7	2	
5	Cap. 47 pF, ceramic, 50 V, NPO	0402	C8, C9	2	(AVX) 04025A470JAT2A
6	Cap. 0.1 µF, ceramic, 16 V, X7R	0603	C4, C5	2	(AVX) 0603YC104KAT2A
7	Resistor, 30.1Ω , 1/16 W, 1%	0402	R4, R5	2	(KOA) RK73H1E30R1F
8	Open	0603	R3	1	
9	Resistor, 49.9 Ω, 1/16 W, 1%	0603	R1, R2	2	(Phycomp) 9C06031A49R9FKRFT
10	Jack, banana receptance, 0.25" dia. hole		J3, J4, J5	3	(HH Smith) 101
11	Test point, red		J6	1	(Keystone) 5000
12	Test point, black		TP1	1	(Keystone) 5001
13	Connector, edge, SMA PCB jack		J1, J2	2	(Johnson) 142-0701-801
14	IC THS4302		U1	1	(TI) THS4302RGT
15	Standoff, 4-40 hex, 0.625" length			4	(Keystone) 1808
16	Screw, phillips, 4-40, 0.250"			4	SHR-0440-016-SN
17	Board, printed-circuit			1	(TI) EDGE # 6443548 Rev. C

ADDITIONAL REFERENCE MATERIAL

- *PowerPAD Made Easy,* application brief (SLMA004)
- *PowerPAD Thermally Enhanced Package,* technical brief (SLMA002)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
THS4302RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4302RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4302RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS4302RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

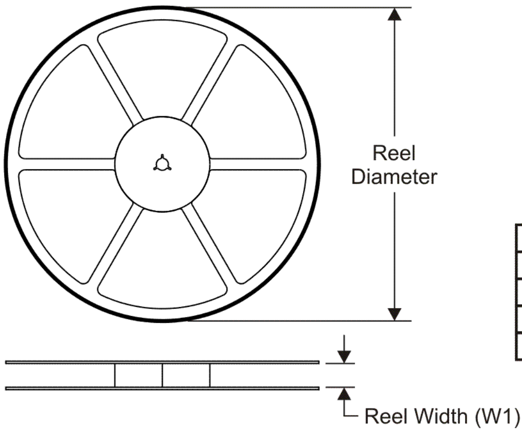
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

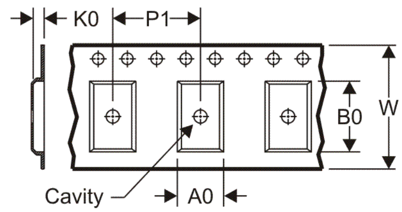
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

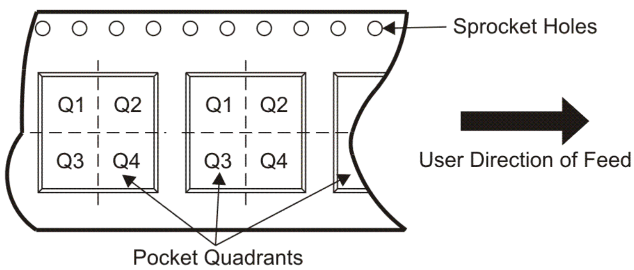


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

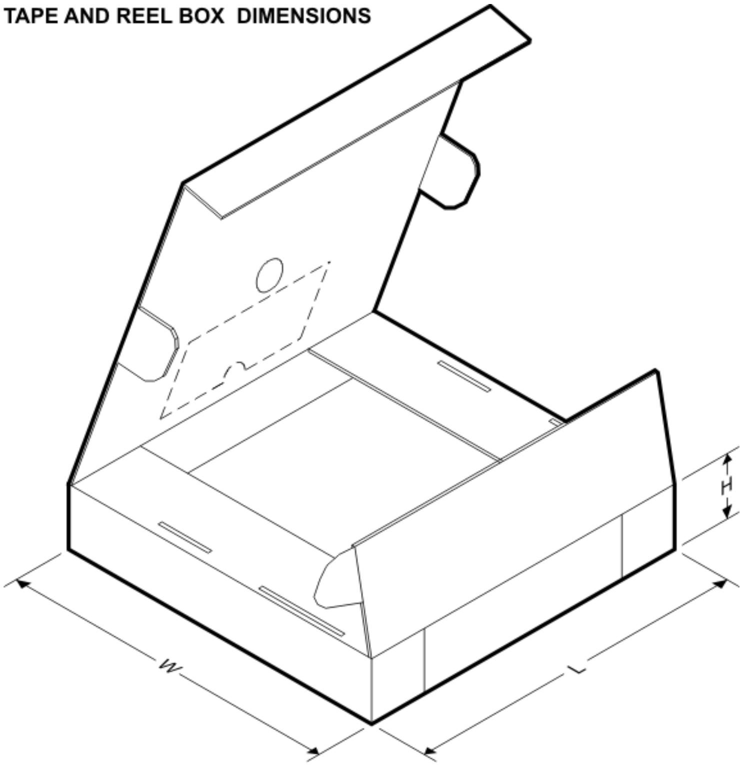
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4302RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS4302RGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

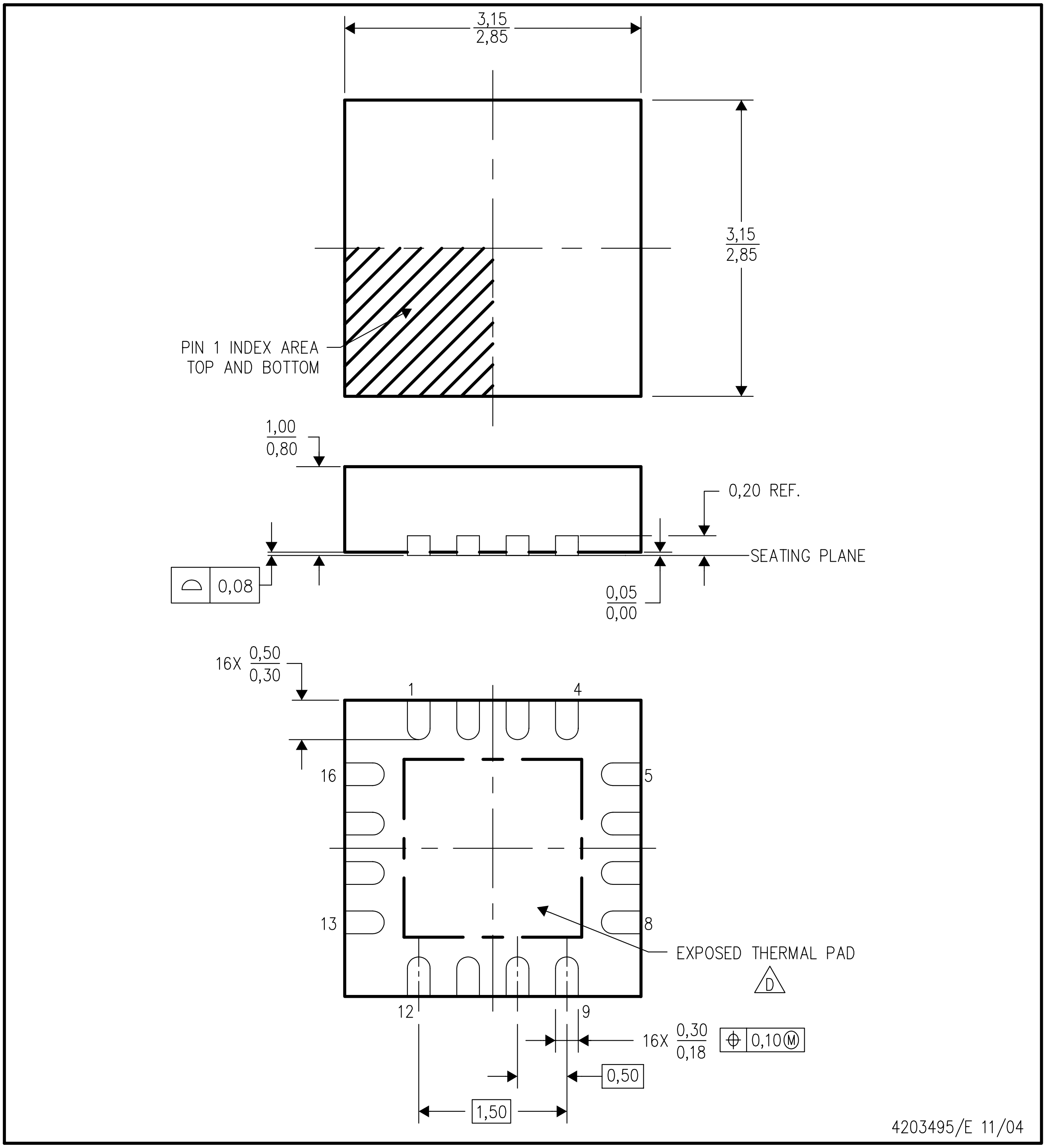
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4302RGTR	QFN	RGT	16	3000	340.5	333.0	20.6
THS4302RGTT	QFN	RGT	16	250	340.5	333.0	20.6

RGT (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

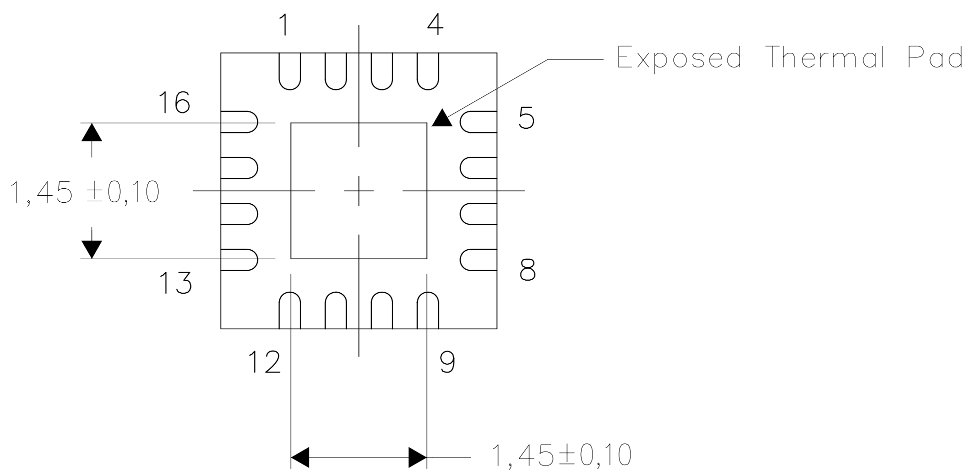
THERMAL PAD MECHANICAL DATA

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

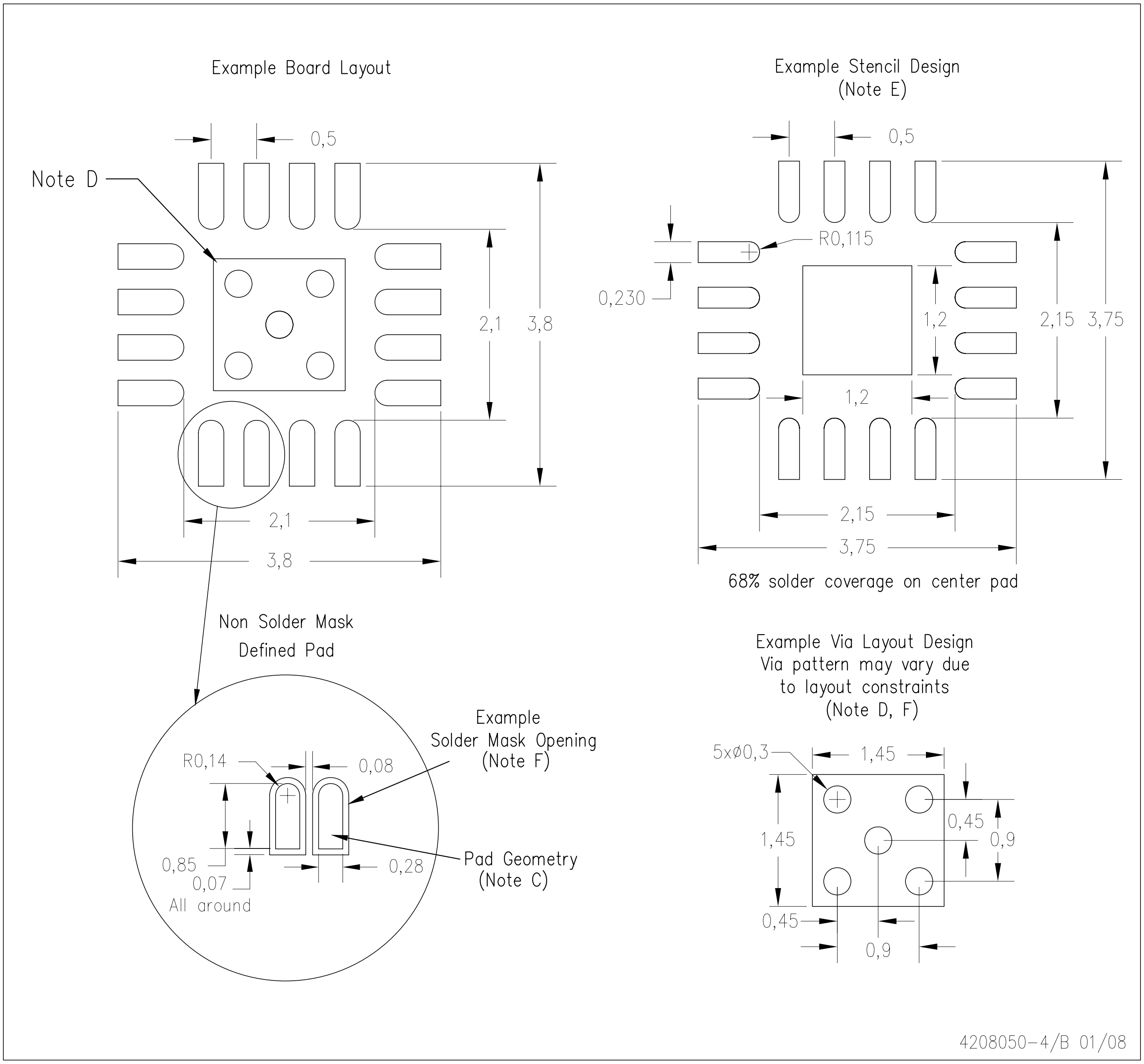


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGT (S-PQFP-N16)



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.